AMENDMENTS TO THE SPECIFICATION

Please amend the specification as indicated below. The language being added is underlined ("__") and the language being deleted contains a strikethrough ("——").

Please substitute the following annotated paragraph for paragraph [0072]:

[0072] Referring now to FIG. 5, yet another exemplary processor instruction for determining a minimum value of a plurality of values is illustrated in accordance with at least one embodiment of the present invention. In some instances, a source register may have the capacity to store two or more values for comparison. For example, a 32-bit source register could be used to store two 16-bit values. Accordingly, in one embodiment, the present invention provides for a processor instruction, herein referred to as the "MIN" instruction", adapted to manipulate a processor to determine, in parallel, the minimum value of two values in a first source register[[s]] and the minimum value of two values in a second source register and store the minimum value of the first source register and the minimum value of the second source register in a destination register. The "MIN" instruction is further adapted to manipulate the processor to store the indexes of the minimum values in another destination register (i.e., the MINDEX register), which preferably includes a special-purpose register. As with the "min" instruction and "Min" instruction discussed above, the "MIN" instruction can be represented in Assembly language format as "MIN rD, rA, rB, index", where rA, rB are the source registers being compared, rD is the destination register, and index is an immediate field having a constant-value index. The performance of the "MIN" instruction by a processor is illustrated by the following instruction flow diagram 500. The "MIN" instruction can be executed in a single cycle using a suitable processor, such as the exemplary network processor illustrated in FIGS. 7 and 8.